Please replace the paragraph beginning at line 9, page 7 with the following rewritten paragraph:

--The core gate stacks are then formed, via step 218. Step 218 preferably includes providing a photoresist mask having apertures over portions of the core 102 which are between the gate stacks and etching the exposed portions of the semiconductor device 100. Figure 4D detects the semiconductor device 100 after step 218 as completed. The gate stacks 110 and 120 have been formed in the core 102. The portions of layers 152', 154', 156', 158' and 160' remain in the periphery 104.--

A3

REMARKS

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Attorney for Applicants

By: _____

Kelly K. Kordzik
Reg. No. 36,571
Robert A. Voigt, Jr.
Reg. No. 47,159

5400 Renaissance Tower
1201 Elm Street
Dallas, Texas 75270-2199
(512) 370-2851

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

The paragraph beginning at line 14, page 5 has been amended as follows:

Figure 2 is a high-level flow chart of one embodiment of a method 200 in accordance with the present invention for providing a semiconductor device having self aligned contacts with a lower sheet resistance. The semiconductor device has a core and a periphery, which are fabricated on a substrate. A plurality of core gate stacks in the core, via step 202. Each of the plurality of core gate stacks includes [including] a first polysilicon gate and a Wsi layer above the first polysilicon gate. Consequently, electrical contact can be made to the first polysilicon gate. In a preferred embodiment, spacers will also be formed at the edges of the fore gate stacks.

The paragraph beginning at line 14, page 6 has been amended as follows:

A first layer of polysilicon that will be used in forming gates and a protective layer are provided over a substrate 101 in both a core region 102 and a periphery 104, via step 212. Figure 4A depicts the semiconductor device 100 after formation of the polysilicon layer 152 and the protective layer 154. The protective layer 154 is preferably made of SiN, SiON or an oxide. The portion of the protective layer that is over the core is then removed to open the core, via step 214. Preferably, step 214 includes providing a photoresist mask that has an aperture over the core 102 and covers the periphery 104. Figure 4B depicts the semiconductor device 100 after step 214 is completed. The polysilicon layer 152 is exposed over the core 102, with a remaining portion 154' [152'] of the protective layer residing over the periphery 104.

The paragraph beginning at line 9, page 7 has been amended as follows:

The core gate stacks are then formed, via step 218. Step 218 preferably includes providing a photoresist mask having apertures over portions of the core 102 which are between the gate stacks and etching the exposed portions of the semiconductor device

100. Figure 4D detects the semiconductor device 100 after step 218 as completed. [Figure 4D] The gate stacks 110 and 120 have been formed in the core 102. The portions layers 152', 154', 156', 158' and 160' remain in the periphery 104.

AUSTIN_1\206017\1
184-G99999